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Sheet	1	of	2
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Complete if Known

Application / Conf. No.	10/624,617 / 6598
Filing Dat	July 21, 2003
First Named Invent r	Michael J. Hart
Art Unit	2819
Examiner Name	Unknown
Attorney Docket Number	X-865-ID US

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

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**Examiner
Signature**

James W Cho

Date Considered

6/2104

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application / C nf. No.	10/624,617 / 6598
		Filing Date	July 21, 2003
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		Examiner Name	Unknown
		Attorney Docket Number	X-865-1D US
Sheet	2	of	2

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>JK</i>		Nose, K. et al.; "V _{TH} -hopping Scheme for 82% Power Saving in Low-Voltage Processors"; Proceedings of the IEEE 2001 Custom Integrated Circuits Conference; May 6-9, 2001; pp. 93-96.	
<i>JK</i>		Kuroda, T. et al.; "A 0.9 V 150 MHz 10 mW 4 mm ² -D Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme"; Solid-State Circuits Conference; 1996; Digest of Technical Papers; 42nd ISSCC; IEEE International; February 8, 1996; pp. 166-167, 437.	
<i>JK</i>		Kuroda, T. et al.; "A High-Speed Low-Power 0.3/sp1 mu/m CMOS Gate Array with Variable Threshold Voltage (VT) Scheme"; Custom Integrated Circuits Conference; 1996; Proceedings of the IEEE 1996; May 5-8 1996; pp. 53-56.	

Examiner Signature	<i>James A. Cho</i>	Date Considered	6/2/04
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